

## REMARKS

### Claim Objections

The Examiner has objected to claims 20 and 22 because of the following informalities: the limitations as recited in claim 20, line 3, include "said second electrical connections having more routing channels extending therefrom than said first electrical connections." The Examiner stated, however, as described in the specification and Figs. 3 and 4, the first electrical connections have more routing channels extending therefrom than those from the second electrical connections. The limitations as recited in claim 22, line 2, include "wherein said first and second electrical connections are positioned on said surface in a progressive pitch layout." The Examiner stated, however, as described in the specification and Figs. 3 and 4, the second plurality of the electrical connections do not have positions having progressively increasing or decreasing spacing.

Claims 20 and 22 have been cancelled.

### 35 U.S.C. § 102 Rejections

The Examiner has rejected claims 15-19 under 35 U.S.C. § 102(b) as being anticipated by Brandenburg.

Claims 15-19 have been cancelled.

New claims 35, 40, and 45 include adjacent rows of electrical connections being spaced progressively further apart from a central region to an outer region of the substrate with no electrical connections between. Specifically, claim 35 includes

the limitation "a space between every pair of adjacent rows of the first plurality of rows is progressively larger from the central region to the outer region to contain a progressively increasing number of conductive traces, said space containing no electrical connections." Claim 40 includes the limitations "a first plurality of rows of electrical connections on said surface, each of said rows extending from the central region to the outer region," "a space between each adjacent row, each of the spaces containing no electrical connections," and "wherein an average of all the spaces is progressively non-decreasing from the central region to the outer region." Claim 45 includes the limitation "a first plurality of rows of electrical connections on said first surface, each of said rows extending from the central region to the outer region, wherein a space between ones of the electrical connections at substantially a same distance from the central region of the first plurality of rows is progressively larger from the central region to the outer region, said space containing no electrical connections."

Brandenburg does not disclose adjacent rows of electrical connections being spaced progressively further apart from a central region to an outer region of the substrate with no electrical connections between. Brandenburg discloses a terminal pattern for an integrated circuit device, such as a ball grid array package or an integrated circuit flip chip (Abstract). As illustrated in Fig. 4, the terminal 26 are arranged in concentric arrays 28a through 28d (col. 5, lines 45-49). The terminal pattern is configured to maximize the density of the individual terminals of the terminal pattern, so as to minimize the maximum width of the terminal pattern (col.

4, lines 51-54). As illustrated in Fig. 4, the terminals 26 may be considered to be arranged in a plurality of rows extending from a central region (array 28d) to an outer region (array 28a). However, as illustrated, as the rows of terminals 26 extend outwards, additional terminals (arrays 28a and 28b) are added such that there are electrical connections between the rows of electrical connections as the rows extend towards the outer portion of the substrate. Specifically, Brandenburg does not disclose adjacent rows of electrical connections being spaced progressively further apart from a central region to an outer region of a substrate with no electrical connections between.

Therefore, claims 35, 40, and 45 are not anticipated by Brandenburg because claims 35, 40, and 45 include limitations that are not disclosed in Brandenburg.

Claims 36-39, 41-44, and 46-48 are dependent on either claim 35, claim 40, or claim 45 and should be allowable for the same reasons as claims 35, 40, and 45 stated above.

#### 35 U.S.C. § 103 Rejections

The Examiner has rejected claims 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Brandenburg in view of Johnson.

Claims 21 and 22 have been cancelled.

New claims 35, 40, and 45 include adjacent rows of electrical connections being spaced progressively further apart from a central region to an outer region of the substrate with no electrical connections between. Specifically, claim 35 includes

the limitation "a space between every pair of adjacent rows of the first plurality of rows is progressively larger from the central region to the outer region to contain a progressively increasing number of conductive traces, said space containing no electrical connections." Claim 40 includes the limitations "a first plurality of rows of electrical connections on said surface, each of said rows extending from the central region to the outer region," "a space between each adjacent row, each of the spaces containing no electrical connections," and "wherein an average of all the spaces is progressively non-decreasing from the central region to the outer region." Claim 45 includes the limitation "a first plurality of rows of electrical connections on said first surface, each of said rows extending from the central region to the outer region, wherein a space between ones of the electrical connections at substantially a same distance from the central region of the first plurality of rows is progressively larger from the central region to the outer region, said space containing no electrical connections."

As previously discussed, Brandenburg does not disclose adjacent rows of electrical connections being spaced progressively further apart from a central region to an outer region of the substrate with no electrical connections between.

Johnson does not teach or suggest adjacent rows of electrical connections being spaced progressively further apart from a central region to an outer region of a substrate with no electrical connections between. Johnson teaches the connection of an integrated circuit chip to a substrate through a pattern of pads arranged in single lines along the radial edged of segments of a polygon underlying the chip-

linear conductors from the pads (Abstract). As clearly illustrated in Figs. 1 and 2, some of the pads are arranged in pairs of rows which are evenly spaced from the central region to the outer region of the substrate. Specifically, Johnson does not teach or suggest adjacent rows of electrical connections being spaced progressively further apart from a central region to an outer region of the substrate with no electrical connections between.

Therefore, claims 35, 40, and 45 are patentable over Brandenburg in view of Johnson because claims 35, 40, and 45 include limitations that are not taught or suggested by Brandenburg and Johnson.

Claims 36-39, 41-44, and 46-48 are dependent on either claim 35, claim 40, or claim 45 and should be allowable for the same reasons as claims 35, 40, and 45 stated above.

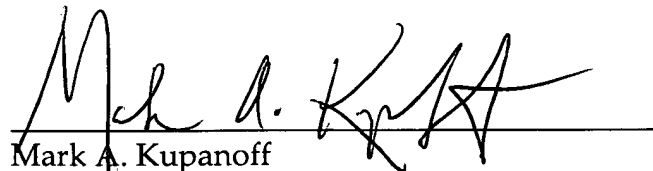
Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Mark A. Kupanoff at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), Applicant hereby requests and authorizes the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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